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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of Daryl D. Starr et al.		Ser. No:	09/675,700
Filing Date:	September 29, 2000	Examiner:	Barbara N. Burgess
Atty. Docket No:	ALA-010B	GAU:	2157

For: INTELLIGENT NETWORK STORAGE INTERFACE DEVICE

January 31, 2008

MS Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF FOR APPELLANT

This is an Appeal of the Final Rejection of claims 1-7 and 21-33 dated September 20, 2007. A Notice of Appeal was mailed by appellants on December 12, 2007 and received by the Patent Office December 17, 2007.

Real Party In Interest

Alacritech, Inc. is the real party in interest.

Related Appeals and Interferences

Appellants know of no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this pending Appeal.

Status of Claims

The application was originally filed with 16 claims. Claims 17-20 were added in an Amendment mailed March 11, 2005. In an Election and Amendment mailed June 31, 2005, appellants canceled claims 8-20 and added new claims 21-33. Claims 1-7 and 21-

33 were finally rejected on September 20, 2007. Pending claims 1-7 and 21-33 are the subject of this Appeal. Appendix A contains a copy of the claims that are involved in this Appeal.

Status of Amendments

No amendments have been filed subsequent to the Final Rejection.

Summary of Claimed Subject Matter[1]

Claim 1 recites an interface device [FIGs. 1, 2, 5, 15, 23, 25: 22; FIG. 5: 303, 310; FIGs. 6, 7, 8, 9: 400; FIG. 9: 490; FIG. 14: 606, 622] for a computer [FIGs. 1, 2, 5, 6, 9, 23, 25: 20; FIG. 14: 600, 602] the interface device connectable to a network [FIGs. 1, 2, 5: 25; FIG. 5: 305, 313, FIG. 6: 414, 416, 418, 420; FIGs. 7, 8: 450; FIG. 9: 414, 416, 418; FIG. 14: 604, 644, 650, 652; FIG. 15: 702, 704, 706, 708; FIG. 23: 2105] and a storage unit [FIGs. 1, 2: 70; FIG. 5: 66, 308, 315; FIG. 7: 462, 464, 466; FIG. 7: 462; FIG. 14: 640, 642], the storage unit including a disk drive [page 8, lines 4, 15, 30; page 18, line 16; page 24, line 4; page 27, line 2; page 28, line 14], the interface device comprising: a sequencer including a hardware logic circuit configured to process a transport layer header of a network packet [FIGs. 1, 2: 52; FIG. 6: 412; FIG. 8: 475; FIG. 10: 502; FIG. 11: 546; FIG. 15: 732, 734, 736, 738; FIG. 23: 732, 2104, 2105; FIG. 24: 2105], a memory adapted to store control information regarding a network connection being handled by said device [FIGs. 1, 2: 74; FIG. 6: 410; FIG. 8: 482; FIG. 10: 508; FIGs. 15, 23: 748], and a mechanism for associating said packet with said control information and for selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer [FIG. 2: 98; page 4, lines 8-15, 22-26; page 5, lines 4-7; page 10, lines 3-11; page 13, lines 3-5; page 14, lines 12-20; page 50, lines 15-17].

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[1] The following summary pursuant to 37 CFR §41.37(c)(1)(v) is a concise explanation of the independent claims and is to be read in light of the disclosure. For conciseness this summary does not list all of the places in the specification and figures that relate to those claims. This summary does not limit the claims (see MPEP §1206).

Independent claim 21 recites an interface device [FIGs. 1, 2, 5, 15, 23, 25: 22; FIG. 5: 303, 310; FIGs. 6, 7, 8, 9: 400; FIG. 9: 490; FIG. 14: 606, 622] for a computer [FIGs. 1, 2, 5, 6, 9, 23, 25: 20; FIG. 14: 600, 602] the interface device connectable to a network [FIGs. 1, 2, 5: 25; FIG. 5: 305, 313, FIG. 6: 414, 416, 418, 420; FIGs. 7, 8: 450; FIG. 9: 414, 416, 418; FIG. 14: 604, 644, 650, 652; FIG. 15: 702, 704, 706, 708; FIG. 23: 2105] and a storage unit [FIGs. 1, 2: 70; FIG. 5: 66, 308, 315; FIG. 7: 462, 464, 466; FIG. 7: 462; FIG. 14: 640, 642], the storage unit including a disk drive [page 8, lines 4, 15, 30; page 18, line 16; page 24, line 4; page 27, line 2; page 28, line 14], the interface device comprising: a receive mechanism that processes a Transmission Control Protocol (TCP) header of a network packet [FIGs. 1, 2: 52; FIG. 6: 412; FIG. 8: 475; FIG. 10: 502; FIG. 11: 546; FIG. 15: 732, 734, 736, 738; FIG. 23: 732, 2105; FIG. 24: 2105], a memory storing a combination of information describing an established TCP connection [FIGs. 1, 2: 74; FIG. 6: 410; FIG. 8: 482; FIG. 10: 508; FIGs. 15, 23: 748], and a processing mechanism that associates said packet with said information and selects whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer [FIG. 2: 98; page 4, lines 8-15, 22-26; page 5, lines 4-7; page 10, lines 3-11; page 13, lines 3-5; page 14, lines 12-20; page 50, lines 15-17].

Independent claim 28 recites a method for operating an interface device [FIGs. 1, 2, 5, 15, 23, 25: 22; FIG. 5: 303, 310; FIGs. 6, 7, 8, 9: 400; FIG. 9: 490; FIG. 14: 606, 622] for a computer [FIGs. 1, 2, 5, 6, 9, 23, 25: 20; FIG. 14: 600, 602], the interface device connectable to a network [FIGs. 1, 2, 5: 25; FIG. 5: 305, 313, FIG. 6: 414, 416, 418, 420; FIGs. 7, 8: 450; FIG. 9: 414, 416, 418; FIG. 14: 604, 644, 650, 652; FIG. 15: 702, 704, 706, 708; FIG. 23: 2105] and a storage unit [FIGs. 1, 2: 70; FIG. 5: 66, 308, 315; FIG. 7: 462, 464, 466; FIG. 7: 462; FIG. 14: 640, 642], the storage unit including a disk drive [page 8, lines 4, 15, 30; page 18, line 16; page 24, line 4; page 27, line 2; page 28, line 14], the method comprising: receiving, by the interface device from the network, a packet containing data and a Transmission Control Protocol (TCP) header [FIG. 3: 100; FIG. 10: 60; FIG. 23; FIG. 24; page 27, lines 4-6, 24-28; page 42, lines 26- 27], processing, by the interface device, the TCP header [FIG. 3: 102; FIG. 10: 502; FIG. 11: 546; FIG. 23; FIG. 24; page 13, lines 15-17; page 21, lines 11-27], storing, on the interface device, information regarding a TCP connection [FIGs 1, 2. 2: 74; FIG. 3: 118;

page 10, lines 16-27; page 11, lines 7-12; page 13, line 25-page 14, line 13; page 15, line 6; page 23, lines 11-23; page 25, line 21; page 26, lines 8-15; page 32, lines 9-13], associating, by the interface device, the packet with the TCP connection [FIG. 3: 110; page 11, lines 15-19; page 13, line 25-page 14, line 1; page 23, lines 21-28; page 48, lines 3-5], and selecting, by the interface device, whether to process the packet by the computer or to send the data from the packet to the storage unit, thereby avoiding the computer [FIG. 3: 106, 110, 114, 120; page 4, lines 24-26; page 5, lines 4-7; page 10, lines 2-11; page 11, line 13-page 12, line 3; page 14, lines 12-20; page 19, lines 20-24; page 22, lines 1-30].

Grounds of Rejection to be Reviewed on Appeal

(1) The rejection of claims 1, 3-4, 6-7, 21, 23-24 and 26-33 under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 6,650,640 Muller et al. (hereinafter "Muller") in view of U.S. Patent No. U.S. Published Application No. 20010048681 to Bilic et al. ("Bilic").

(2) The rejection of claims 2, 5, 22 and 25 under 35 U.S.C. §103(a) as allegedly being unpatentable over Muller in view of Bilic and in further view of U.S. Patent No. 6,065,096 to Day.

Argument

I. Regarding Grounds of Rejection (1), appellants demonstrate below that the Final Rejection is deficient in two primary ways. First, the Final Rejection ignores certain claim limitations. Second, the Final Rejection points to features in the reference documents that do not disclose the limitations of the claims. In short, the Final Rejection fails to present a *prima facie* case of obviousness, as explained in the detailed analysis below.

A. Claim 1

Regarding claim 1, the Final Rejection states, on pages 2 and 3:

> Claims 1, 3-4, 6-7, 21, 23-24, 26-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (hereinafter "Muller", 6,650,640 B1) in view of Bilic et al. (hereinafter "Bilic", US Patent Publication 20010048681 Al).

As per claim 1, Muller discloses an interface device for a computer, the interface device connectable to a network and a storage unit, the storage unit including a disk drive, the interface device comprising:

- A sequencer including a hardware logic circuit configured to process a transport layer header of a network packet (column 4, lines 48-50, column 7, lines 20-25, 31-35, 64-67, column 8, lines 1-5, 17-20, 50-60, column 9, lines 1-5, column 15, lines 35-38, column 35, lines 53-67, column 36, lines 11-30);
- A memory adapted to store control information regarding a network connection being handled by said device (column 4, lines 20-25, column 9, lines 14-16, 20-25, 56-58, column 10, lines 1-7, column 11, lines 46-59, column 12, lines 11-15, column 52, lines 64-67, column 53, lines 1-7;
- A mechanism for associating said packet with said control information (column 4, lines 45-50, 58-67, column 8, lines 50-60, 66-67, column 9, lines 13-17, 22-35, 66-67, column 10, lines 2-7, column 11, lines 46-59, column 12, lines 11-15, column 16, lines 59-67).

Muller does not explicitly disclose:

- selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer.

However, in an analogous art, Bilic discloses a protocol processor arranged to select the group of packets for reassembly depending on which of the communication protocols was used in transmitting the packets. It controls the host interface logic so to write the data packets that do not belong to the identified group to the host memory without reassembly processing by the network interface device (paragraphs [0013, 0023, 0026, 0043, 0046]).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate Bilic's selecting whether to process packet or send to storage, thereby avoiding the computer in Muller's system to reduce the burden of frame reassembly imposed on the host processor.

The Final Rejection admits that Muller does not disclose "selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer." Appellants respectfully assert that Bilic also does not disclose this limitation. Note that claim 1, for example, includes the limitation of "the storage unit including a disk drive." None of the paragraphs of Bilic cited by the Final Rejection teach or suggest "selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer," wherein "the storage unit includ(es) a disk drive." Instead, as noted in paragraph [0013]

of Bilic, "In some preferred embodiments of the present invention, the embedded processor is programmed to process TCP/IP and UDP/IP headers, and thus to reassemble TCP and UDP frames (or segments) in the host memory. Packets transferred using other protocols are passed through to the host processor without header processing or reassembly."

In other words, in contrast with the limitation of "selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer," Bilic does not even suggest that packets transferred using different protocols go to different memories, but rather states that all the packets go to the host memory, albeit with different processing. That is, Bilic does not teach or suggest that certain packets "avoid... the computer," as recited in claim 1. Beyond that, Bilic certainly does not teach or suggest that data from a packet are sent to "a storage unit, the storage unit including a disk drive," as recited in claim 1. Because neither Muller nor Bilic teach or suggest "a mechanism for ... selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer," appellants respectfully assert that claim 1 and all the claims that depend from claim 1 are nonobvious over Muller in view of Bilic.

Beginning on page 10 of the Final Rejection, the Examiner provides a "Response to Arguments" section that explains the Examiner's position with regard to the above argument. The Examiner states, on pages 11 and 12:

> In response to applicant's arguments, the recitation "storage unit including a disk drive has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478,481 (CCPA 1951).

Applicants do not disagree with these early cases. Indeed, it is clear from the explanation of the cases given by the Examiner that the preamble should be considered a limitation of the present case, because it provides antecedent basis for the other limitations found in the "body of the claim," which therefore depend on the preamble.

Moreover, a more thorough explanation of whether a preamble should be viewed as a limitation, found in *Catalina Mktg. Int'l v. Coolsavings,com, Inc.*, 289 F.3d 801, 808-809 (Fed. Cir. 2002), buttresses the finding that the preamble at issue in present claims should be given patentable weight. For example, as noted in *Catalina* at 808, "dependence on a particular disputed preamble phrase for antecedent basis may limit claim scope because it indicates a reliance on both the preamble and claim body to define the claimed invention. *Bell Communications Research, Inc. v. Vitalink Communications Corp.*, 55 F.3d 615, 620, 34 USPQ2d 1816, 1820 (Fed. Cir. 1995)." As can easily be seen, each of the independent claims has a preamble that provides antecedent support for the "claim body."

In addition, as stated in *Catalina* at 808-809, "clear reliance on the preamble during prosecution to distinguish the claimed invention from the prior art transforms the preamble into a claim limitation because such reliance indicates use of the preamble to define, in part, the claimed invention. See generally *Bristol-Myers Squibb Co. v. Ben Venue Labs.*, Inc., 246 F.3d 1368, 1375, 58 USPQ2d 1508, 1513 (Fed. Cir. 2001)." Applicants have amended independent claim 1 to add limitations to the preamble of that claim, added similar limitations to the preambles of new independent claims 21 and 28, and have argued that the preamble is a limitation in each of the independent claims, clearly relying upon those preambles to define the invention. This reliance on the preamble is a demonstration of "what the inventors actually invented and intended to encompass by the claim." *Catalina* at 808.

For these reasons, it is clear that the preamble should be considered a limitation of the independent claims. The Examiner does not dispute applicants' arguments that Bilic does not disclose the limitations of the preamble. Instead, the Examiner states that "the recitation 'storage unit including a disk drive' has not been given patentable weight because the recitation occurs in the preamble." According to the authority and reasons discussed above, it is clear that the preamble provides a limitation to claim 1 not found in the cited art, and that the Final Rejection has failed to present a *prima facie* case of obviousness by ignoring this limitation.

B. Claim 3

Regarding claim 3, the Final Rejection states:

> As per claim 3, Muller discloses the interface device of claim 1, further comprising a plurality of network ports, wherein one of the said network ports is connectable to the storage unit (column 4, lines 40-43, column 6, lines 37-40, column 7, lines 15-19, column 8, lines 40-43, column 9, lines 1-5, column 10, lines 65-67).

Appellants have reviewed the passages from Muller that the Final Rejection cites regarding claim 3 and respectfully assert that none of those passages teaches or suggests "The interface device of claim 1, further comprising a plurality of network ports, wherein one of said network ports is connectable to the storage unit." For example, column 4, lines 40-43 (and surrounding text) of Muller state:

> Illustratively, a flow key comprises a combination of identifiers of the source and destination entities. In one embodiment of the invention a flow key is a combination of source and destination addresses extracted from the packet's layer three (e.g., IP or Internet Protocol) protocol header and source and destination port numbers extracted from the layer four (e.g., TCP) protocol header.

Appellants respectfully assert that the "port numbers" mentioned in Muller are numbers rather than physical elements, and as such cannot be connected to a storage unit. Because neither Muller nor Bilic teach or suggest "The interface device of claim 1, further comprising a plurality of network ports, wherein one of said network ports is connectable to the storage unit," the Final Rejection has not presented a *prima facie* case of obviousness for claim 3.

C. Claim 4

Regarding claim 4, the Final Rejection states:

> As per claim 4, Muller discloses the interface device of claim 1, further comprising a Fibre Channel controller connectable to the storage unit (column 61, lines 55-60).

Instead, column 61, lines 55-60 of Muller states:

> Reserving sixty-four bytes at the beginning of a buffer also allows header information to be modified or prepended if necessary. For example, a regular Ethernet header of a packet may, because of routing requirements, need to be replaced with a much larger FDDI (Fiber

Distributed Data Interface) header. One skilled in the art will recognize the...

Appellants respectfully assert that the above-quoted passage that was cited by the Final Rejection does not teach or suggest "the interface device of claim 1, further comprising a Fibre Channel controller connectable to the storage unit," as recited in claim 4. For at least this reason, the Final Rejection has not presented a *prima facie* case of obviousness for claim 4.

D. Claim 6

Regarding claim 6, the Final Rejection states:

> As per claim 6, Muller discloses the network interface device of claim 1, further comprising a file cache adapted to store said data (column 56, lines 20-30, column 58, lines 26-30, column 61, lines 34-35, column 62, lines 47-52).

Appellants have reviewed the passages from Muller that the Final Rejection cites regarding claim 6, and have reprinted them below for the Board's convenience. Column 56, lines 20-30 of Muller state:

> Free ring manager 1012 attempts to ensure that a buffer is always available for a packet. Thus, in one embodiment of the invention free ring manager 1012 includes descriptor cache 1012a configured to store a number of descriptors (e.g., up to eight) at a time. Whenever there are less than a threshold number of entries in the cache (e.g., five), additional descriptors may be retrieved from the free descriptor ring. Advantageously, the descriptors are of such a size (e.g., sixteen bytes) that some multiple (e.g., four) of them can be efficiently retrieved in a sixty-four byte cache line transfer from the host computer.

Column 58, lines 26-30 (and surrounding text) of Muller state:

> A packet's completion descriptor may be marked appropriately when the buffer identified by its buffer identifier is to be released to the host computer. For example, a flag may be set in the descriptor to indicate that the packet's buffer is being released from DMA engine 120 to the host computer or software operating on the host computer (e.g., a driver associated with NIC 100). In one embodiment of the invention, completion ring manager 1014 includes completion descriptor cache 1014a. Completion descriptor cache 1014a may store one or more completion descriptors for collective transfer from DMA engine 120 to the host computer.

Column 61, lines 34-35 (and surrounding text) of Muller state:

> In another alternative embodiment of the invention, a second level of padding may be added to each entry in a buffer that stores non-re-assembled packets that are larger than 256 bytes (e.g., MTU packets and jumbo packets that are not split). In this alternative embodiment, a cache line of storage (e.g., sixty-four bytes for a Solaris™ workstation) is skipped in the buffer before storing each packet. The extra padding area may be used by software that processes the packets and/or their completion descriptors. The software may use the extra padding area for routing or as temporary storage for information needed in a secondary or later phase of processing.

Column 62, lines 47-52 (and surrounding text) of Muller state:

> In another embodiment the free ring manager extracts descriptors from the free descriptor ring and stores them in a descriptor cache until a buffer is needed, at which time the buffer's buffer identifier is stored in the free buffer array. In yet another embodiment, a descriptor may be used (e.g., the buffer that it references may be used to store a packet) while still in the cache.

It is clear that that none of those passages teaches or suggests "...a file cache adapted to store said data." For at least this reason, the Final Rejection has not presented a *prima facie* case of obviousness for claim 6.

E. Claim 7

Regarding claim 7, the Final Rejection states:

> As per claim 7, Muller further discloses the interface device of claim 1, further comprising a file cache adapted to store said data under control of a file system in the host (column 56, lines 20-30, column 58, lines 26-30, column 61, lines 34-35, column 62, lines 47-52).

The passages cited by the Final Rejection are reprinted above. It is clear that that none of those passages teaches or suggests "...a file cache adapted to store said data under control of a file system in the host." For at least this reason, the Final Rejection has not presented a *prima facie* case of obviousness for claim 7.

F. Claim 21

Regarding claim 21, the Final Rejection states:

> As per claim 21, Muller discloses an interface device for a computer, the interface device connectable to a network and a storage unit, the storage unit including a disk drive, the interface device comprising:
>
> - A receive mechanism that processes a Transmission Control Protocol (TCP) header of a network packet (column 4, lines 48-50,

column 7, lines 20-25, 31-35, 64-67, column 8, lines 1-5, 17-20, 50-60, column 9, lines 1-5, column 15, lines 35-38, column 35, lines 53-67, column 36, lines 11-30);

- A memory storing a combination of information describing an established TCP connection (column 4, lines 20-25, column 9, lines 14-16, 20-25, 56-58, column 10, lines 1-7, column 11, lines 46-59, column 12, lines 11-15, column 52, lines 64-67, column 53, lines 1-7);
- A processing mechanism that associates said packet with said information (column 4, lines 45-50, 58-67, column 8, lines 50-60, 66-67, column 9, lines 13-17, 22-35, 66-67, column 10, lines 2-7, column 11, lines 46-59, column 12, lines 11-15, column 16, lines 59-67).

Muller does not explicitly disclose:

- selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer.

However, in an analogous art, Bilic discloses a protocol processor arranged to select the group of packets for reassembly depending on which of the communication protocols was used in transmitting the packets. It controls the host interface logic so to write the data packets that do not belong to the identified group to the host memory without reassembly processing by the network interface device (paragraphs [0013, 0023, 0026, 0043, 0046]).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate Bilic's selecting whether to process packet or send to storage, thereby avoiding the computer in Muller's system to reduce the burden of frame reassembly imposed on the host processor.

The Final Rejection admits that Muller does not disclose "selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer." Appellants respectfully assert that Bilic also does not disclose this limitation. Note that claim 21, for example, includes the limitation of "the storage unit including a disk drive." None of the paragraphs of Bilic cited by the Final Rejection teach or suggest "selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer," wherein "the storage unit includ(es) a disk drive." Instead, as noted in paragraph [0013] of Bilic, "In some preferred embodiments of the present invention, the embedded processor is programmed to process TCP/IP and UDP/IP headers, and thus to reassemble TCP and UDP frames (or segments) in the host memory. Packets transferred using other

protocols are passed through to the host processor without header processing or reassembly."

In other words, in contrast with the limitation of "selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer," Bilic does not even suggest that packets transferred using different protocols go to different memories, but rather states that all the packets go to the host memory, albeit with different processing. That is, Bilic does not teach or suggest that certain packets "avoid... the computer," as recited in claim 21. Beyond that, Bilic certainly does not teach or suggest that data from a packet are sent to "a storage unit, the storage unit including a disk drive," as recited in claim 21. Because neither Muller nor Bilic teach or suggest "a mechanism for ... selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer," appellants respectfully assert that claim 21 and all the claims that depend from claim 21 are nonobvious over Muller in view of Bilic.

G. Claim 23

Regarding claim 23, the Final Rejection states:

> As per claim 23, Muller discloses the interface device of claim 21, further comprising a Fibre Channel controller connectable to the storage unit (column 61, lines 55-60).

Appellants initially note that claim 23 recites:

> The interface device of claim 21, further comprising a plurality of network ports, wherein one of said network ports is connectable to the storage unit.

In contrast, column 61, lines 55-60 of Muller recite:

> Reserving sixty-four bytes at the beginning of a buffer also allows header information to be modified or prepended if necessary. For example, a regular Ethernet header of a packet may, because of routing requirements, need to be replaced with a much larger FDDI (Fiber Distributed Data Interface) header. One skilled in the art will recognize the...

Appellants respectfully assert that the above-quoted passage that was cited by the Final Rejection does not teach or suggest "the interface device of claim 21, further comprising a plurality of network ports, wherein one of said network ports is connectable

to the storage unit," as recited in claim 23. For at least this reason, the Final Rejection has not presented a *prima facie* case of obviousness for claim 23.

H. Claim 24

Regarding claim 24, the Final Rejection states:

> As per claim 24, Muller discloses the network interface device of claim 1, further comprising a file cache adapted to store said data (column 56, lines 20-30, column 58, lines 26-30, column 61, lines 34-35, column 62, lines 47-52).

Appellants initially note that claim 24 recites:

> The interface device of claim 21, further comprising a Fibre Channel controller connectable to the storage unit.

Appellants respectfully assert that the passages from Muller that the Final Rejection cites regarding claim 24, which are reprinted above with regard to claim 6, do not teaches or suggests "the interface device of claim 21, further comprising a Fibre Channel controller connectable to the storage unit." Nor does the passage of Muller cited by the Final Rejection with regard to claim 23 (column 61, lines 55-60, reprinted above with regard to claim 23) teach or suggest the limitations of claim 24. For at least these reasons, the Final Rejection has not presented a *prima facie* case of obviousness for claim 24.

I. Claim 26

Regarding claim 26, the Final Rejection states:

> As per claim 26, Muller discloses the network interface device of claim 21, further comprising a file cache adapted to store said data (column 56, lines 20-30, column 58, lines 26-30, column 61, lines 34-35, column 62, lines 47-52).

The passages from Muller that the Final Rejection cites regarding claim 26 are reprinted above with regard to claim 6. Appellants respectfully assert that none of those passages teaches or suggests "the interface device of claim 21, further comprising a file cache adapted to store said data." Instead, some of those passages teach a cache for descriptors. For at least this reason, the Final Rejection has not presented a *prima facie* case of obviousness for claim 26.

J. Claim 27

Regarding claim 27, the Final Rejection states:

> As per claim 27, Muller discloses the network interface device of claim 21, further comprising a file cache adapted to store said data under control of a file system in the host (column 56, lines 20-30, column 58, lines 26-30, column 61, lines 34-35, column 62, lines 47-52).

The passages from Muller that the Final Rejection cites regarding claim 27 are reprinted above with regard to claim 6. Appellants respectfully assert that none of those passages teaches or suggests "The interface device of claim 21, further comprising a file cache adapted to store said data under control of a file system in the host." For at least this reason, the Final Rejection has not presented a *prima facie* case of obviousness for claim 27.

K. Claim 28

Regarding claim 28, the Final Rejection states:

> As per claim 28, Muller discloses a method for operating an interface device for a computer, the interface device connectable to a network and a storage unit, the storage unit including a disk drive, the method comprising:
>
> - Receiving, by the interface device from the network, a packet containing data and a Transmission Control Protocol (TCP) header (column 4, lines 48-50, column 7, lines 20-25, 31-35, 64-67, column 8, lines 1-5, 17-20, 50-60, column 9, lines 1-5, column 15, lines 35-38, column 35, lines 53-67, column 36, lines 11-30);
> - Processing, by the interface device, the TCP header (column 4, lines 45-50, 58-67, column 8, lines 50-60, column 9, lines 13-17, 22-35, 66-67);
> - Storing, on the interface device, information regarding a TCP connection (column 4, lines 20-25, column 9, lines 14-16, 20-25, 56-58, column 10, lines 1-7, column 11, lines 46-59, column 12, lines 11-15);
> - Associating, by the interface device, the packet with the TCP connection (column 35, lines 53-67, column 36, lines 11-30);
>
> Muller does not explicitly disclose:
>
> - Selecting, by the interface device, whether to process the packet by the computer or to send the data from the packet to the storage unit, thereby avoiding the computer.
>
> However, in an analogous art, Bilic discloses a protocol processor arranged to select the group of packets for reassembly depending on which of the communication protocols was used in transmitting the packets. It controls the host interface logic so to write the data packets that do not

belong to the identified group to the host memory without reassembly processing by the network interface device (paragraphs [0013, 0023, 0026, 0043, 00461).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate Bilic's selecting whether to process packet or send to storage, thereby avoiding the computer in Muller's system to reduce the burden of frame reassembly imposed on the host processor.

The Final Rejection admits that Muller does not disclose "selecting, by the interface device, whether to process the packet by the computer or to send the data from the packet to the storage unit, thereby avoiding the computer." Appellants respectfully assert that Bilic also does not disclose this limitation. Note that claim 28, for example, includes the limitation of "the storage unit including a disk drive." None of the paragraphs of Bilic cited by the Final Rejection teach or suggest "selecting, by the interface device, whether to process the packet by the computer or to send the data from the packet to the storage unit, thereby avoiding the computer." Instead, as noted in paragraph [0013] of Bilic, "In some preferred embodiments of the present invention, the embedded processor is programmed to process TCP/IP and UDP/IP headers, and thus to reassemble TCP and UDP frames (or segments) in the host memory. Packets transferred using other protocols are passed through to the host processor without header processing or reassembly."

In other words, Bilic does not even suggest that packets transferred using different protocols go to different memories, but rather states that all the packets go to the host memory, albeit with different processing. That is, Bilic does not teach or suggest that certain packets "avoid... the computer," as recited in claim 28. Beyond that, Bilic certainly does not teach or suggest that data from a packet are sent to "a storage unit, the storage unit including a disk drive," as recited in claim 28. Because neither Muller nor Bilic teach or suggest "selecting, by the interface device, whether to process the packet by the computer or to send the data from the packet to the storage unit, thereby avoiding the computer," appellants respectfully assert that claim 28 and all the claims that depend from claim 28 are nonobvious over Muller in view of Bilic.

L. Claim 29

Regarding claim 29, the Final Rejection states:

As per claim 29, Muller discloses the method of claim 28, further comprising creating, by the computer, the information regarding the TCP connection (column 5, lines 35-45).

Column 5, lines 35-45 of Muller state:

> FIG. 7 is a flow chart demonstrating one method of distributing the processing of network packets among multiple processors on a host computer in accordance with an embodiment of the invention.
>
> FIG. 8 is a diagram of a packet queue for a network interface circuit in accordance with an embodiment of the invention.
>
> FIG. 9 is a diagram of a control queue for a network interface circuit in accordance with an embodiment of the invention.

Appellants respectfully assert that column 5, lines 35-45 of Muller does not teach or suggest "the method of claim 28, further comprising creating, by the computer, the information regarding the TCP connection." For at least this reason, the Final Rejection has not presented a *prima facie* case of obviousness for claim 29.

M. Claim 30

Regarding claim 30, the Final Rejection states:

> As per claim 30, Muller discloses the method of claim 28, wherein the interface device includes a network port, and the packet is received via the port and the data is sent to the storage unit via the port (column 10, lines 1-7).

Column 10, lines 1-7 of Muller state:

> In addition to storing the packet in a packet queue, a corresponding entry for the packet is made in control queue 118 and information concerning the packet's flow may also be passed to dynamic packet batching module 122. Control queue 118 contains related control information for each packet in packet queue 116.

Appellants respectfully assert that column 10, lines 1-7 of Muller do not teach or suggest "the method of claim 28, wherein the interface device includes a network port, and the packet is received via the port and the data is sent to the storage unit via the port." For at least this reason, the Final Rejection has not presented a *prima facie* case of obviousness for claim 30.

N. Claim 31

Regarding claim 31, the Final Rejection states:

> As per claim 31, Muller discloses the method of claim 28, wherein

the interface device includes first and second network ports, and the packet is received via the first port and the data is sent to the storage unit via the second port (column 10, lines 35-47).

Column 10, lines 35-47 (and surrounding text) of Muller state:

> For example, if the checksum calculated by checksum generator 114 was not calculated on the correct portion of the packet, the checksum may be adjusted to capture the correct portion. This adjustment may be made by software operating on a host computer system (e.g., a device driver). Checksum generator 114 may be omitted or merged into another module of NIC 100 in an alternative embodiment of the invention.
>
> From the information obtained by header parser 106 and the flow information managed by flow database manager 108, the host computer system served by NIC 100 in the illustrated embodiment is able to process network traffic very efficiently. For example, data portions of related packets may be re-assembled by DMA engine 120 to form aggregations that can be more efficiently manipulated.

Appellants respectfully assert that it is clear that column 10, lines 35-47 of Muller do not teach or suggest "the method of claim 28, wherein the interface device includes first and second network ports, and the packet is received via the first port and the data is sent to the storage unit via the second port." For at least this reason, the Final Rejection has not presented a prima *facie case* of obviousness for claim 31.

O. Claim 32

Regarding claim 32, the Final Rejection states:

> As per claim 32, Muller discloses the method of claim 28, further comprising storing the data on a file cache of the interface device (column 56, lines 20-30, column 58, lines 26-30, column 61, lines 34-35, column 62, lines 47-52).

The passages from Muller that the Final Rejection cites regarding claim 32 are reprinted above with regard to claim 6. Appellants respectfully assert that none of those passages teaches or suggests "The method of claim 28, further comprising storing the data on a file cache of the interface device." For at least this reason, the Final Rejection has not presented a prima *facie case* of obviousness for claim 32.

Regarding claim 33, the Final Rejection states:

> As per claim 33, discloses the method of claim 28, further comprising adding a network protocol header to the data for sending the data to the storage unit (column 9, lines 50-67).

In contrast, column 9, lines 50-67 (and surrounding text) of Muller recite:

> By sending all packets in one communication flow or end-to-end connection to a single processor, the correct ordering of packets can be enforced. Load distributor 112 may be omitted in one alternative embodiment of the invention. In another alternative embodiment, header parser 106 may also communicate directly with other modules of NIC 100 besides the load distributor and flow database manager.
>
> Thus, after header parser 106 parses a packet FDBM 108 alters or updates FDB 110 and load distributor 112 identifies a processor in the host computer system to process the packet. After these actions, the header parser passes various information back to IPP module 104. Illustratively, this information may include the packet's flow key, an index of the packet's flow within flow database 110, an identifier of a processor in the host computer system, and various other data concerning the packet (e.g., its length, a length of a packet header).
>
> Now the packet may be stored in packet queue 116, which holds packets for manipulation by DMA (Direct Memory Access) engine 120 and transfer to a host computer.

Appellants respectfully assert that this passage does not teach or suggest "The method of claim 28, further comprising adding a network protocol header to the data for sending the data to the storage unit." For at least this reason, the Final Rejection has not presented a *prima facie* case of obviousness for claim 33.

P. Allegation that Appellants' Argument do not Comply with 37 CFR 1.111

The Final Rejection states, on page 12:

> Appellant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Appellants respectfully assert that their prior reply was fully responsive. Throughout the course of this application, appellants respectfully assert that the Examiner has repeatedly, in multiple prior Office Actions as well as in the Final Rejection, alleged that features were found in reference documents that were not, in actuality, disclosed in those documents. Appellants have merely pointed out the deficiencies in those rejections, because the Office Actions and the Final Rejection have failed to present a *prima facie* rejection for anticipation or obviousness.

II. Regarding Grounds of Rejection (2), the Final Rejection states:

> Claims 2, 5, 22, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (hereinafter "Muller", 6,650,640 B1) in view of Bilic et al. (hereinafter "Bilic", US Patent Publication 20010048681 A1) and in further view of Day et al. (hereinafter "Day", US Patent 6065096).

A. Claims 2 and 22

Regarding claims 2 and 22, the Final Rejection states:

> As per claims 2 and 22, Muller, in view of Bilic, discloses the interface device of claims 1 and 21.
> Muller, in view of Bilic, does not explicitly disclose the interface further comprising a SCSl controller connectable to the storage unit.
> However, Day discloses SCSl interface channels attached to disk drives (column 2, lines 40-54, column 5, lines 1-25).
>
> Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate in Muller's device Day's interface comprising a SCSl controller in order to provide for a simple, lower cost RAID controller architecture to enable lower cost and complexity associated with high performance and high reliability storage subsystems.

As noted above regarding claim 1, Muller in view of Bilic does not teach or suggest "a mechanism ... for selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer." Similarly, regarding claim 21, Muller in view of Bilic does not teach or suggest "a processing mechanism that ... selects whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer." Day also does not teach or suggest either of these limitations. Implementing or incorporating in Muller's device Day's interface as proposed by the Final Rejection would not solve this deficiency.

Moreover, the motivation asserted by the Final Rejection to make this modification is quoted from Day at column 2, lines 51-54, which refers to an alternative storage configuration, not anything involving network communication. Appellants respectfully assert, however, that somehow implementing or incorporating in Muller's device Day's interface would increase the cost and complexity of Muller's device without any obvious benefit. Muller's device "relates to a network interface circuit (NIC) for

processing communication packets exchanged between a computer network and a host computer system" (column 1, lines 51-54). Day's RAID controller, on the other hand, provides a chip for controlling a redundant array of inexpensive disk drives (column 1, lines 11-19; column 2, lines 11-24). Stated differently, Muller involves network communication and Day involves storage. Absent the teachings of the present invention, no motivation is apparent in the cited references to make the modification proposed by the Final Rejection. For at least these reasons, appellants respectfully assert that the Final Rejection has not presented a *prima facie* case of obviousness for claims 2 or 22.

B. Claims 5 and 25

Regarding claims 5 and 25, the Final Rejection states:

> As per claims 5 and 25, Muller, in view of Bilic, discloses the interface device of claims 1 and 21.
>
> Muller, in view of Bilic, does not explicitly disclose the interface further comprising a RAID controller connectable to the storage unit.
>
> However, Day discloses a RAID controller that integrates onto a single integrated circuit of a general purpose processor (column 2, lines 11-25, 55-67).
>
> Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate in Muller's device Day's interface comprising a RAID controller allowing the disk interface connections and protocols to be more flexibly selected but at the cost of less integration within the circuit.

As noted above regarding claim 1, Muller in view of Bilic does not teach or suggest "a mechanism ... for selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer." Similarly, as noted above regarding claim 21, Muller in view of Bilic does not teach or suggest "a processing mechanism that ... selects whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer." Day also does not teach or suggest either of these limitations. Implementing or incorporating in Muller's device Day's interface as proposed by the Final Rejection would not solve this deficiency.

Moreover, the motivation asserted by the Final Rejection to make this modification is quoted from Day at column 2, lines 51-54, which refers to an alternative storage configuration, not anything involving network communication. As mentioned

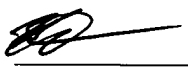
above, somehow implementing or incorporating in Muller's device Day's interface would increase the cost and complexity of Muller's device without any obvious benefit. Muller's device "relates to a network interface circuit (NIC) for processing communication packets exchanged between a computer network and a host computer system" (column 1, lines 51-54). Day's RAID controller, on the other hand, provides a chip for controlling a redundant array of inexpensive disk drives (column 1, lines 11-19; column 2, lines 11-24). Stated differently, Muller involves network communication and Day involves storage. Absent the teachings of the present invention, no motivation is apparent in the cited references to make the modification proposed by the Final Rejection. For at least these reasons, appellants respectfully assert that the Final Rejection has not presented a *prima facie* case of obviousness for claims 5 or 25.

Conclusion

As detailed above, the Final Rejection fails to state a *prima facie* case of obviousness for any of the pending claims. Appellants respectfully assert that all the pending claims are allowable and requests reversal of the Examiner's rejections.

This brief is being submitted along with a check in the amount of $510.00 to pay the Appeal Brief Fee.

Respectfully submitted,



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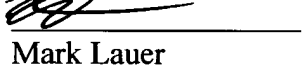

Mark Lauer

APPENDIX A – CLAIMS APPENDIX

1. An interface device for a computer, the interface device connectable to a network and a storage unit, the storage unit including a disk drive, the interface device comprising:

a sequencer including a hardware logic circuit configured to process a transport layer header of a network packet,

a memory adapted to store control information regarding a network connection being handled by said device, and

a mechanism for associating said packet with said control information and for selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer.

2. The interface device of claim 1, further comprising a SCSI controller connectable to the storage unit.

3. The interface device of claim 1, further comprising a plurality of network ports, wherein one of said network ports is connectable to the storage unit.

4. The interface device of claim 1, further comprising a Fibre Channel controller connectable to the storage unit.

5. The interface device of claim 1, further comprising a RAID controller connectable to the storage unit.

6. The interface device of claim 1, further comprising a file cache adapted to store said data.

7. The interface device of claim 1, further comprising a file cache adapted to store said data under control of a file system in the computer.

21. An interface device for a computer, the interface device connectable to a network and a storage unit, the storage unit including a disk drive, the interface device comprising:

a receive mechanism that processes a Transmission Control Protocol (TCP) header of a network packet,

a memory storing a combination of information describing an established TCP connection, and

a processing mechanism that associates said packet with said information and selects whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer.

22. The interface device of claim 21, further comprising a SCSI controller connectable to the storage unit.

23. The interface device of claim 21, further comprising a plurality of network ports, wherein one of said network ports is connectable to the storage unit.

24. The interface device of claim 21, further comprising a Fibre Channel controller connectable to the storage unit.

25. The interface device of claim 21, further comprising a RAID controller connectable to the storage unit.

26. The interface device of claim 21, further comprising a file cache adapted to store said data.

27. The interface device of claim 21, further comprising a file cache adapted to store said data under control of a file system in the computer.

28. A method for operating an interface device for a computer, the interface device connectable to a network and a storage unit, the storage unit including a disk drive, the method comprising:

receiving, by the interface device from the network, a packet containing data and a Transmission Control Protocol (TCP) header,

processing, by the interface device, the TCP header,

storing, on the interface device, information regarding a TCP connection,

associating, by the interface device, the packet with the TCP connection, and

selecting, by the interface device, whether to process the packet by the computer or to send the data from the packet to the storage unit, thereby avoiding the computer.

29. The method of claim 28, further comprising creating, by the computer, the information regarding the TCP connection.

30. The method of claim 28, wherein the interface device includes a network port, and the packet is received via the port and the data is sent to the storage unit via the port.

31. The method of claim 28, wherein the interface device includes first and second network ports, and the packet is received via the first port and the data is sent to the storage unit via the second port.

32. The method of claim 28, further comprising storing the data on a file cache of the interface device.

33. The method of claim 28, further comprising adding a network protocol header to the data for sending the data to the storage unit.

APPENDIX B – EVIDENCE APPENDIX

No evidence is being submitted by appellants, and so there is no need for this appendix. Appellants' attorney has, however, received a Notice of Non-Compliant Appeal Brief in an unrelated case for failing to provide such an unnecessary appendix, and so appellants provide this appendix to avoid that objection.

APPENDIX C – RELATED PROCEEDINGS APPENDIX

Appellants know of no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this pending Appeal, and so there is no need for this appendix. Appellants' attorney has, however, received a Notice of Non-Compliant Appeal Brief in an unrelated case for failing to provide such an unnecessary appendix, and so appellants provide this appendix to avoid that objection.